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EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 05/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/840,306	MIZUNO ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 April 2001* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/734,218*.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4)☐ Interview Summary (PTO-413) Paper No(s). _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Response to Arguments

2. Applicant's arguments with respect to claims 1 – 44 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 5, 6, 20, 22, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa, JP 05024976; Stirn, US 4,596,645 and Booske, US 5,672,541 in view of Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2,Chapter 2, Lattice Press, 1990.

Regarding claims 1, 5, 20 and 24, Nakagawa teaches a fabrication method for semiconductor devices such as diode and transistor (see English Abstract and the English translation of the article) by the process of plasma sputtering comprising the steps of:

- holding the semiconductor substrate 105 in the vacuum chamber (see Fig. 1) in and the impurity solid including impurity target 109 to be introduced into the diode or the transistor formation region in the vacuum chamber 101(see Fig. 1);
- introducing an inert/noble gas in to generate the plasma;
- applying a first voltage to the impurity solid target to serve as a cathode 104 for the plasma, performing sputtering and thereby mixing the impurity from the solid target into the plasma in various places of the disclosure (see English translation);
- applying a second voltage 103 to the semiconductor substrate so that the impurity mixed with the plasma is introduced directly to the surface portion of the device formation region to form an impurity layer (region 34 in Fig. 3).

Nakagawa fails to teach:

1) the second voltage allowing the semiconductor substrate to serve as cathode.

2) forming an inter connection layer to electrically connect the impurity layer, and

3) electrically isolating the diode or the transistor formation region on the substrate by an element isolation layer.

Regarding 1), Stirn teaches that substrate can be biased with a negative voltage during sputtering in column 5, lines 32 – 37 to control the stress level in the film.

Regarding 2), Booske teaches forming an inter connection layer to electrically connect the impurity layer in column 13, lines 45 – 57 as shown in Fig. 6.

Regarding 3) Nakagawa, Stirn and Booske fail to teach electrically isolating the diode or the transistor formation region on the substrate by an element isolation layer.

Wolf discloses in Chapter 2 that device isolation is necessary when fabricating ICs so that the devices can subsequently be interconnected to create desired circuit configurations.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify the method of Nakagawa and bias the substrate with negative voltage to control film stress as taught by Stirn and form the inter connection layer to electrically connect the impurity layer as taught by Booske to complete the device and electrically isolate the diode or the transistor formation region on the substrate by some form of an element isolation layer as taught by Wolf so that the devices can subsequently be interconnected to create desired circuit configurations.

Regarding claims 3 and 22, both Stirn and Booske teaches use of impurity gases for reactive sputtering process and will therefore produce impurity layers containing components from the reactive impurity gas (see Booske in column 3, lines 6 – 14).

Regarding claims 6 and 25, Nakagawa, Stirn and Booske teach silicon substrate and Nakagawa and Booske teach impurity of B and P (see Booske in column 5, lines 27 – 34 and reactive gas including Ar in (see Booske column 8, line 27).

5. Claims 2 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa, JP 05024976; Stirn, US 4,596,645 and Booske, US 5,672,541 in view of Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2,Chapter 2, Lattice Press, 1990 as applied to claims 1 and 20 above, and further in view of Yamazaki, US 5,789,292.

Nakagawa teaches a doping method, which includes irradiation of an ultraviolet radiation on the semiconductor substrate (see the claims).

Nakagawa, Stirn and Booske in view of Wolf fail to teach irradiation of a laser beam on the semiconductor substrate.

Yamazaki teaches a method of laser doping in which laser beam is irradiated on the substrate on the semiconductor substrate (see abstract of the disclosure).

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to form the device by irradiating a laser beam at an ultraviolet wave length on the semiconductor substrate as taught by Yamazaki instead of the ultraviolet light taught by Nakagawa since the doping process can be better controlled by controlling the laser radiation.

6. Claims 4 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa, JP 05024976; Stirn, US 4,596,645 and Booske, US 5,672,541 in view of Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2,Chapter 2, Lattice Press, 1990 as applied to claims 3 and 22 above, and further in view of Zhang, US 5,320,984.

Nakagawa, Stirn and Booske in view of Wolf fail to teach the concentration of the components of the inert gas exceeding 1×10^{20} cm^{-3}.

Zhang teaches doping the target with impurity concentration higher than 1×10^{17} $atoms.cm^{-3}$ in column 3, lines 24 – 25.

Therefore, it would have been obvious to one with ordinary skill in the art at the

time of the invention to generate a concentration of the components of the inert gas of Nakagawa's method exceeding 1 X 10^{20} cm^{-3} as taught by Zhang since this level of concentration will be necessary for proper doping of the substrate.

7. Claims 7, 9, 11, 12, 13, 26, 28, 30, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa, JP 05024976 and Booske, US 5,672,541 in view of Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2,Chapter 2, Lattice Press, 1990.

Regarding claims 7 and 26, Nakagawa and Booske in view of Wolf teach most of the limitations of these claims as has been explained above with respect to claims 1 and

Nakagawa teaches a method of semiconductor doping in which the first voltage to the impurity target serves as cathode (104 in Fig. 1) and the second voltage applied to the substrate serving as anode (103 in Fig. 1).

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify the method of Nakagawa and Booske by electrically isolating the diode or the transistor formation region on the substrate by some form of an element isolation layer as taught by Wolf so that the devices can subsequently be interconnected to create desired circuit configurations..

Regarding claims 9 and 28, Booske teaches impurity layers containing components from the reactive impurity gas in column 3, lines 6 – 14.

Regarding claims 11, 12, 30 and 31, Nakagawa teaches negative voltages for the target and Booske teaches negative voltages for the substrate as was explained above in rejecting claims 1 and 20 (see Booske, column 11, lines 28 – 30).

Regarding claims 13 and 32, Booske teaches silicon substrate in column 8, line 40, impurity of B and P in column 5, lines 27 – 34 and reactive gas including Ar in column 8, line 27. Nakagawa also teaches similar limitations 9see English Abstract).

8. Claims 8 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa, JP 05024976 and Booske, US 5,672,541 in view of Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2,Chapter 2, Lattice Press, 1990 as applied to claims 7 and 26 above, and further in view of Yamazaki, US 5,789,292.

Nakagawa and Booske in view of Wolf teach a doping method, which includes irradiation of an ultraviolet radiation on the semiconductor substrate (see Nakagawa's claims).

Nakagawa and Booske in view of Wolf fail to expressly teach irradiation of a laser beam on the semiconductor substrate.

Yamazaki teaches a method of laser doping in which laser beam is irradiated on the substrate on the semiconductor substrate (see abstract of the disclosure).

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to form the device by irradiating a laser beam at an ultraviolet wave length on the semiconductor substrate as taught by Yamazaki instead of the ultraviolet light taught by Nakagawa since the doping process can be better controlled by controlling the laser radiation.

Claims 10 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa, JP 05024976 and Booske, US 5,672,541 in view of Wolf, Silicon

Processing for the VLSI Era by Wolf, Vol. 2,Chapter 2, Lattice Press, 1990 as applied to claims 9 and 28 above, and further in view of Zhang, US 5,320,984.

Nakagawa and Booske in view of Wolf fail to teach the concentration of the components of the inert gas exceeding 1 X 10^{20} cm^{-3}.

Zhang teaches doping the target with impurity concentration higher than 1 X 10^{17} $atoms.cm^{-3}$ in column 3, lines 24 – 25.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to generate a concentration of the components of the inert gas of Nakagawa and Booske's method exceeding 1 X 10^{20} cm^{-3} as taught by Zhang since this level of concentration will be necessary for proper doping of the substrate.

9. Claims 14, 16, 18, 19, 33, 35, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa, JP 05024976; Stirn, US 4,596,645 and Booske, US 5,672,541 in view of and Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2,Chapter 2, Lattice Press, 1990.

Regarding claims 14 and 33, Nakagawa, Stirn and Booske in view of Wolf teach most of the limitations of these claims as has been explained above with respect to claims 1, 7 20 and 26.

Stirn also teaches a sputtering process from an impurity target in which the targets are biased to attract negatively ionized inert gas (see the abstract of the disclosure).

Stirn fails to teach applying a positive potential to the target to serve it as an anode.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to form the device as taught by Nakagawa by the use of an apparatus where the substrate is kept at a positive potential as taught by Nakagawa and the target is kept at a positive potential since negatively charged ions of the plasma will be attracted by the positively charged target for sputtering impurity ions from the target.

Regarding claims 16 and 35, Booske teaches impurity layers containing components from the reactive impurity gas in column 3, lines 6 – 14.

Regarding claims 18 and 37, Booske teaches negative voltages for both the target and the substrate as was explained above in rejecting claims 1 and 20.

Regarding claims 19 and 38, Booske teaches silicon substrate in column 8, line 40, impurity of B and P in column 5, lines 27 – 34 and reactive gas including Ar in column 8, line 27.

10. Claims 15 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa, JP 05024976; Stirn, US 4,596,645 and Booske, US 5,672,541 in view of and Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2,Chapter 2, Lattice Press, 1990 as applied to claims 14 and 33 above, and further in view of Yamazaki, US 5,789,292.

Nakagawa, Stirn and Booske in view of Wolf teach a doping method, which Includes irradiation of an ultraviolet radiation on the semiconductor substrate (see Nakagawa's claims).

Yamazaki teaches a method of laser doping in which laser beam is irradiated on the substrate on the semiconductor substrate (see abstract of the disclosure).

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to form the device by irradiating a laser beam at an ultraviolet wave length on the semiconductor substrate as taught by Yamazaki instead of the ultraviolet light taught by Nakagawa since the doping process can be better controlled by controlling the laser radiation.

11. Claims 17 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa, JP 05024976; Stirn, US 4,596,645 and Booske, US 5,672,541 in view of and Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2,Chapter 2, Lattice Press, 1990 as applied to claims 16 and 35 above, and further in view of Zhang, US 5,320,984.

Nakagawa, Stirn and Booske in view of Wolf fail to teach the concentration of the components of the inert gas exceeding 1×10^{20} cm^{-3}.

Zhang teaches doping the target with impurity concentration higher than 1×10^{17} $atoms.cm^{-3}$ in column 3, lines 24 – 25.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to generate a concentration of the components of the inert gas of Nakagawa and Booske's method exceeding 1×10^{20} cm^{-3} as taught by Zhang since this level of concentration will be necessary for proper doping of the substrate.

12. Claims 39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa, JP 05024976; Stirn, US 4,596,645 and Booske, US 5,672,541 in view

of and Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2,Chapter 2, Lattice Press, 1990.

Regarding these claims, Stirn teaches a separate power supply 41 for the substrate and a separate power supply 36 for the sputtering targets.

12. Claims 40 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa, JP 05024976; Stirn, US 4,596,645 and Booske, US 5,672,541 in view of and Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2,Chapter 2, Lattice Press,.

The same reasoning as applied above in rejecting claims 39 and 42 can also be used to reject these claims.

13. Claims 41 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa, JP 05024976; Stirn, US 4,596,645 and Booske, US 5,672,541 in view of and Wolf, Silicon Processing for the VLSI Era by Wolf, Vol. 2,Chapter 2, Lattice Press, 1990.

The same reasoning as applied above in rejecting claims 39 and 42 can also be used to reject these claims.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 703 308 2521. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 703 308 1233. The fax phone numbers

for the organization where this application or proceeding is assigned are 703 308 7722 for regular communications and 703 308 7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 4918.

Asok K. Sarkar
May 21, 2003